REMARKS/ARGUMENTS

This Preliminary Amendment accompanies the filing of a Continuation Application of Application Serial No. 10/036,889. In the last action on the merits in the parent case, Office Action dated December 26, 2001, the Examiner: (1) rejected claims 1-3, 5-6, 17, 19-20, 23-24, 27-28, 32-34, 39-41, 44, 49-50 and 53 under 35 U.S.C. § 102(a) as allegedly anticipated by U.S. Patent No. 6,229,363 *(Eto et al.)*; (2) rejected claims 45 and 54 under 35 U.S.C. § 103(a) as allegedly unpatentable over *Eto et al.* in view of U.S. Patent No. 6,184,753 (*Ishimi et al.*); and (3) objected to claims 4, 7-16, 18, 21-22, 25-26, 29-31, 35-38, 42-43, 46-48, 51-52 and 54-61 as allegedly dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

Applicants file a continuation application and Preliminary Amendment to prosecute the claims 1-3, 5-6, 17, 19-20, 23-24, 27-28, 32-34, 39-41, 44-45, 49-50 and 53-54, the non-allowed claims of the parent case. Thus, with this Preliminary Amendment, Applicants cancel claims 4, 7-16, 18, 21-22, 25-26, 29-31, 35-38, 42-43, 46-48, 51-52 and 54-61 in favor of those same claims in the parent case. Applicants believe the pending claims are allowable over the art of record and respectfully request reconsideration.

I. Amendment to the Specification

The amendments presented to the specification are merely to document this application's relationship to the parent application, Serial No. 10/036,889. Applicants respectfully submit that no new matter is submitted thereby.

II. Claim Rejections

A. Claim 1

The Examiner rejected claim 1 as allegedly anticipated by *Eto et al.* Claim 1 is a method that requires defining a time window between features of a first and second reference clock signals, and comparing a target clock signal to the reference clock signals.

The Examiner makes specific citations to *Eto et al.* and asserts that the *Eto et al.* reference teaches all the limitations of claim 1. The assertion is respectfully traversed based on the following remarks. *Eto et al.* teaches a semiconductor device that uses a "first clock phase adjusting circuit for adjusting

the phase of an external clock and generating an internal clock." *Eto* Col. 5, lines 34-36. In addition, *Eto et al.* teaches the use of a "second clock phase adjusting circuit for controlling the phase of the internal clock signal." *Eto* Col. 5, lines 36-39. The first clock phase adjusting circuit is used to "conform [the external clock] with the phase of the internal clock," and the second clock phase adjusting circuit is used for "controlling the phase of the internal clock signal with higher accuracy than the first clock phase adjusting circuit." *Eto* Col. 5, lines 36-37; Col. 6, lines 42-44. *Eto et al.* does not teach, suggest, or even imply defining a time window between features of a first and second reference clock signals, as required in claim 1.

Second, *Eto et al.* teaches that the "phase comparisons between the external clock signal and the internal clock signal in the first and second clock phase shift circuits 1 and 2 are carried out **mutually independent**." *Eto* Col. 10, lines 46-50 (emphasis added). Thus, *Eto et al.* does not teach, suggest, or even imply the comparing of the target (*i.e.,* the external) clock signal to the reference (*i.e.,* the internal) clock signals, as required by claim 1.

Based on the foregoing, Applicants respectfully submit that claim 1, and all claims which depend from claim 1 (Claims 2-3), should be allowed.

B. Claim 5

The Examiner rejected claim 5 as allegedly anticipated by *Eto et al.* Claim 5 is directed to a system that requires a clock domain region having a target clock; and a jitter measurement circuit associated with the clock domain region that measures an uncertainty window.

Eto et al. teaches a semiconductor device that uses a first and second clock phase adjusting circuit to adjust the phase of an external clock, generate an internal clock, and control the phase of the generated internal clock signal. *Eto* Col. 5, lines 34-39. The first and second clock phase adjusting circuits are carried out mutually independent and are used to conform the external clock to the phase of the internal clock, not for measuring an uncertainty window. *Eto* Col. 5, lines 36-40; Col. 10, lines 46-50. *Eto et al.* does not teach, suggest, or even imply a jitter measurement circuit that measures an uncertainty window within which a cache clock makes state transitions, as required in claim 5.

Based on the foregoing, Applicants respectfully submit that claim 5, and all claims which depend from claim 5 (Claim 6 and 17), should be allowed.

C. Claim 19

Claim 19 is a method that requires defining a time window between features of a first and second reference clock signals, and comparing a target clock signal to the reference clock signals.

The Examiner makes specific citations to *Eto et al.* and asserts that the *Eto et al.* reference teaches all the limitations of claim 19. The assertion is respectfully traversed based on the following remarks. First, *Eto et al.* teaches a semiconductor device that uses a first and second clock phase adjusting circuit to adjust the phase of an external clock, generate an internal clock, and control the phase of the generated internal clock signal. *Eto* Col. 5, lines 34-39. The first and second clock phase adjusting circuits are carried out mutually independent and are used to conform the external clock to the phase of the internal clock, not for defining a time window. *Eto* Col. 5, lines 36-40; Col. 10, lines 46-50. Thus, *Eto et al.* does not teach, suggest, or even imply the defining of a time window between features of a first and second reference clock signals, as required in claim 19.

Second, Applicants respectfully submit that the cited location in *Eto et al.* does not teach comparing the target clock signal to the reference clock signals.

Based on the foregoing, Applicants respectfully submit that claim 19, and all claims which depend from claim 19 (Claims 20 and 23), should be allowed.

D. Claim 27

Claim 27 is a system that requires a plurality of reference clock signals that define a plurality of time windows between corresponding features of the reference clock signals that are used to determine a uncertainty window of the target clock signal.

The Examiner makes specific citations to *Eto et al.* and asserts that the *Eto et al.* reference teaches all the limitations of claim 27. The assertion is respectfully traversed based on the following remarks. *Eto et al.* teaches conforming the external clock to the phase of the internal clock, not for defining a plurality of time windows. *Eto* Col. 5, lines 36-40; Col. 10, lines 46-50.

Based on the foregoing, Applicants respectfully submit that claim 27, and claims 28 which depend from claim 27, should be allowed.

E. Claim 32

Claim 32 is dependent from claim 27 and further requires a microcontroller adapted to execute software algorithms by way of a scan chain. The Examiner rejected claim 32 as allegedly anticipated by *Eto* et al. *Eto* et al. does not teach, suggest, or even imply the use of scan chain communications to execute software algorithms. Thus, claim 32 is allowable for at least this reason and the same reasons as base claim 27.

F. Claim 39

Claim 39 is a microprocessor that requires a cache region having a cache clock and a measurement means on the microprocessor die for determining skew and jitter of the cache clock. The Examiner rejected claim 39 as allegedly anticipated by *Eto* et al.

Eto et al. teaches a semiconductor device that uses a first and second clock phase adjusting circuit to adjust the phase of an external clock, generate an internal clock, and control the phase of the generated internal clock signal. *Eto* Col. 5, lines 34-39. The first and second clock phase adjusting circuits are carried out mutually independent and are used to conform the external clock to the phase of the internal clock, not for determining skew and jitter. *Eto* Col. 5, lines 36-40; Col. 10, lines 46-50.

In addition, *Eto et al.* teaches a semiconductor that includes "a clock buffer 101 for latching the clock signal (that is, the **external** clock signal) as the reference" *Eto* Col. 14, lines 55-58. (emphasis added). Thus, *Eto et al.* does not teach, suggest, or even imply defining a plurality of time windows between corresponding features of the reference clock signals, or using a cache region having a cache clock.

Based on the foregoing, Applicants respectfully submit that claim 39, and all claims which depend from claim 39 (Claims 40, 41, and 44), should be allowed.

G. Claim 45

Claim 45 is a method that requires defining a first time bin between respective features of the first and second reference clock signals. The Examiner rejected claim 45 as allegedly anticipated by *Eto* et al.

The Examiner makes specific citations to *Eto et al.* and asserts that the *Eto et al.* reference teaches all the limitations of claim 39. The assertion is respectfully traversed. First, *Eto et al.* teaches a semiconductor device that uses a first and second clock phase adjusting circuit to adjust the phase of an external clock, generate an internal clock, and control the phase of the generated internal clock signal. *Eto* Col. 5, lines 34-39. The first and second clock phase adjusting circuits are carried out mutually independent and are used to conform the external clock to the phase of the internal clock, not for defining a time bin. *Eto* Col. 5, lines 36-40; Col. 10, lines 46-50. Thus, *Eto et al.* does not teach, imply, or even suggest defining a first time bin between respective features of the first and second reference clock signals, as required in claim 45.

Based on the foregoing, Applicants respectfully submit that claim 45, and all claims which depend from claim 45 (Claims 49-50), should be allowed.

H. Claim 53

Claim 53 is a microprocessor that requires a cache region having a cache clock, and a measurement circuit that measures an uncertainty window within which the cache clock makes state transitions. The Examiner rejected claim 53 as allegedly anticipated by *Eto* et al.

The Examiner asserts that the *Eto et al.* reference teaches all the limitations of claim 39. The Applicants respectfully traverse this rejection. Eto et al. teaches conforming the external clock to the phase of the internal clock. *Eto* Col. 5, lines 36-40; Col. 10, lines 46-50. *Eto* et al. does not teach, suggest, or even imply measuring an uncertainty window within which the cache clock makes state transitions.

Based on the foregoing, Applicants respectfully submit that claim 53 should be allowed.

III. CONCLUSION

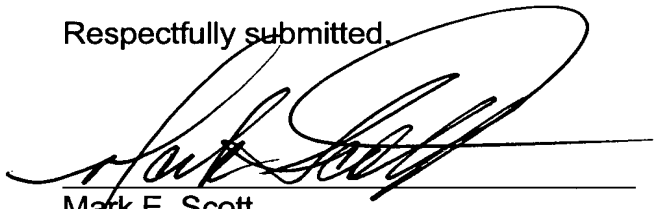
Applicants respectfully request reconsideration and allowance of the pending claims. If the Examiner feels that a telephone conference would expedite the resolution of this case, he is respectfully requested to contact the undersigned.

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the prior art which have yet to be raised, but which may be raised in the future.

If any fees or time extensions are inadvertently omitted or if any fees have been overpaid, please appropriately charge or credit those fees to Hewlett-Packard Company Deposit Account Number 08-2025 and enter any time extension(s) necessary to prevent this case from being abandoned.

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,



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